REMARKS

The Office Action of October 29, 2004 has been received and its contents reviewed. Claims 1 and 75-101 were pending for consideration prior to the Office Action. By this Amendment, claims 1 and 77-80 are amended, claims 75-76, 85-86, and 91-92 are canceled, and claim 102 is added. Support for these amendments can be found throughout the specification, for example, on page 25, lines 17-21, and in Fig. 5D. Accordingly, claims 1, 77-84, 87-90, and 93-102 are pending, of which claims 1 and 77-80 are independent. In view of the following remarks, reconsideration and allowance of the application is respectfully requested.

As is shown in pages 2-3 of the Office Action, claims 75-76, 85-86, and 91-92 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,793,344 to Koyama. Applicants submit that this rejection is moot in light of the cancellation of claims 75-76, 85-86, and 91-92 herein. Thus, Applicants respectfully request that this rejection be withdrawn.

As is shown on pages 3-4 of the Office Action, claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over JP 11-154714 to Yamazaki et al. and U.S. Patent 5,656,845 to Akbar. Applicants respectfully traverse.

In particular, the Office asserts that all features of Claim 1 are disclosed in any one of Yamazaki and Akbar, and that it is obvious to combine the features of Yamazaki and Akbar. In response, claim 1 is amended herein to recite a nonvolatile memory comprising a memory cell array including a plurality of memory cells being formed in a matrix, wherein at least one of the memory cells comprises a memory thin film transistor, and a switching thin film transistor, wherein said memory thin film transistor comprises a first semiconductor active layer over an insulating surface, a floating gate electrode adjacent to the first semiconductor active layer with a first insulating film therebetween, and control gate electrode adjacent to the floating gate with a second insulating film therebetween, wherein said switching thin film transistor comprises a second semiconductor active layer over the insulating surface, and a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween, wherein the first semiconductor active layer and the second semiconductor active layer are in a common semiconductor island, wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second

semiconductor active layer of the switching thin film transistor, and wherein a channel forming region in the first semiconductor active layer is formed by a self-aligning manner using the floating gate as a mask. Neither Yamazaki nor Akbar discloses this feature.

Furthermore, it would not have been obvious to a person of ordinary skill in the art at the time the invention was made to add the novel feature of the channel forming region to the nonvolatile memory based on the teachings of Yamazaki and Akbar, either alone or in combination. In particular, the claimed feature that "the first semiconductor active layer and the second semiconductor active layer are in a common semiconductor island" is helpful to reduce the size of the nonvolatile memory. However, when the common semiconductor island has been used for downsizing, the processing accuracy is a limiting factor in the next step of downsizing. Therefore, claim 1 further includes the feature that "a channel forming region in the first semiconductor active layer is formed by a self-aligning manner using the floating gate as a mask" to enable a reduction of the size of the nonvolatile memory without increasing the limit of the processing accuracy is enabled.

The surprising synergy achieved by the invention by incorporating a "self-aligning manner" with "the common semiconductor island" is unexpected and would not have been obvious to a person of ordinary skill in the art at the time of the invention. Accordingly, Applicants believe that the teachings of Yamazaki et al. and Akbar, neither alone nor in combination, render the invention recited in claim 1 obvious under 35 U.S.C. 103(a). Therefore, Applicants respectfully request that the rejection of claim 1 be withdrawn.

As is shown on pages 4-5 of the Office Action, the Office states that "claims 77 to 84, 97 to 90 and 93 to 96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. and Akbar, as applied to claim 75 and 76 above, and in further view of Koyama." While it is clear that the Office has rejected claims 77-84 and 93-96, it is unclear what is meant by "97 to 90" as is stated in the Office Action. In addition, it is unclear what is meant by the claims being "unpatentable over Yamazaki et al. and Akbar, as applied to claim 75 and 76 above," since Akbar was not applied to a rejection of claims 75 and 76 previously in the Office Action. Accordingly, Applicants respectfully request clarification in these regards.

Addressing features of claims 77-84, 87-90, and 93-96, each of claims 77-80 recite, in part, a semiconductor device wherein a first semiconductor active layer and a second

semiconductor active layer are in a common semiconductor island, and wherein a channel forming region in the first semiconductor active layer is formed by a self-aligning manner using a floating gate as a mask. None of Yamazaki, Akbar, or Koyama, taken either alone or in combination, discloses these features. As described above, the surprising synergy achieved by the invention by incorporating a "self-aligning manner" with "the common semiconductor island" is unexpected and would not have been obvious to a person of ordinary skill in the art at the time of the invention.

Accordingly, Applicants believe that the teachings of Yamazaki et al., Akbar, and Koyama, taken either alone or in combination, fail to render the invention recited in claims 77-80 unpatentable under 35 U.S.C. 103(a), if this is the intended combination in the Office Action. Therefore, Applicants respectfully request that the rejection of claims 77-84, 87-90, and 93-96 be allowed.

As is shown on page 5 of the Office Action, claims 97-101 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al., Akbar, and Koyama, as applied to claims 1, and 77-80 above, and in further view of U.S. Patent 5,627,088 to Fukaya et al. Applicants respectfully traverse.

As stated above, each of claims 1 and 77-80 recite, in part, a semiconductor device wherein a first semiconductor active layer and a second semiconductor active layer are in a common semiconductor island, and wherein a channel forming region in the first semiconductor active layer is formed by a self-aligning manner using a floating gate as a mask. The teachings of Yamazaki et al., Akbar, and Koyama, taken either alone or in combination, fail to teach these features, and thus, fail to render the invention recited in claims 1, and 77-80 unpatentable under 35 U.S.C. 103(a). The teachings of Fukaya et al. also fail to teach these novel features. Accordingly, by virtue of their dependencies on claims 1 and 77-80, claims 97-101 also contain these features.

Therefore, Applicants submit that the teachings of Yamazaki et al., Akbar, and Koyama, taken either alone or in combination, fail to render the invention recited in claims 97-101 unpatentable under 35 U.S.C. 103(a). Thus, Applicants respectfully request that the rejection of claims 97-101 under 35 U.S.C. § 103(a) be withdrawn.

As is shown on pages 6-7 of the Office Action, claims 1 and 75-96 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being

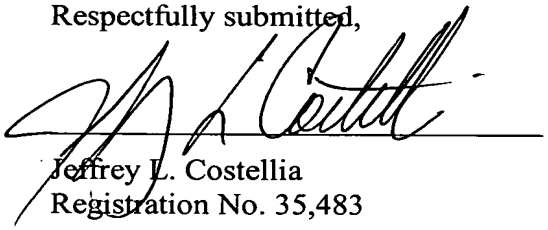
unpatentable over claims 1 to 12 of U.S. Patent No. 6,472,684. Applicants respectfully request that these rejections be held in abeyance until an indication of allowable subject matter is provided.

As is shown on pages 7-8 of the Office Action, claims 1 and 75-96 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 to 30 of U.S. Patent No. 6,509,602. Applicants respectfully request that these rejections be held in abeyance until an indication of allowable subject matter is provided.

In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,



Jeffrey L. Costellia
Registration No. 35,483

NIXON PEABODY LLP
Suite 900, 401 9th Street, N.W.
Washington, D.C. 20004-2128
(202) 585-8000